IJIRSET

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Optimized Routing and Component Placement to Improve the Continuity And Uniformity of the PCB-PIFL Antenna's Co-Planar Ground Plane to Achieve an Overall Improved Antenna Performance

SegeraDavies[1], MwangiMbuthia[2]

P.G. Student, Department of Electrical Engineering, University of Nairobi,Nairobi, Kenya[1]

Associate Professor, Department of Electrical Engineering, University of Nairobi, Nairobi, Kenya[2]

ABSTRACT : A ground plane forms the other half for quarter wave PCB antennas. Integration of these type of antennas with other components within the same PCB of a mobile device compromise the uniformity and continuity of the ground plane due to the requirement for dense routing and component mounting to optimize the use of the limited PCB space available. This will not only detune the matching and introduce losses to the antenna, but also degrade the antenna's performance in terms of gain, bandwidth, efficiency and radiation pattern. To address this issue, this paper presents a case study of an optimized components placement and stacking, effective PCB partitioning, routing discipline combined with right selection of antenna location to achieve a successful integration of a PCB-PIFL antenna into a mixed multilayer PCB design, which provides improved continuity and uniformity of the antenna's co-planar ground plane, and the antenna's and improves the overall performance. The results obtained show that the lower and upper bandwidths determined at -10dB is over 60MHz and 130MHz with return losses of -30dB and -14dB at resonant frequencies 915MHz and 1.931GHz.

KEYWORDS: PCB, Inverted-FL antenna, Bandwidth, GSM,

I. INTRODUCTION

The current demand for mobile devices is more functionality and small form factor. From a PCB design perspective, it implies reduced PCB size, dense routing and crowded component placement. This poses a great challenge to the integration of unbalanced embedded antennas like PIFAs that couple with the ground plane to achieve high radiation performance[1]. If a PIFA antenna is used on a very small PCB, with a small area of copper as the ground plane, its efficiency will degrade and it will be difficult to tune it. Moreover components and PCB tracks introduce additional losses and affect the feed point impedance [2]. To increase the radiation emission and achieve greater bandwidth, the ground plane must be moved away from the microstrip element which makes the fringing field cover more distance. But moving it too far, then the fringing field stops altogether and there no radiation. Therefore, the position and size of the ground plane is vital in the design of a good radiator[3]. Thus it is evident that the size, uniformity and continuity, and the proximity of the ground plane is key to proper functioning of embedded PIFA antennas.

This paper is a case study of the integration of a GSM dual-band inverted-FL antenna into a (120x80) mm PCB for an 8 layer mobile device with optimized routing and component placement to improve the continuity and uniformity of the antenna's co-planar ground plane to achieve an overall improved antenna performance.

II. RELATED WORK

Desirable electrical characteristics of radio frequency(RF) circuit and its PCB layout include low noise, low distortion, low crosstalk and low radiated emissions [1,2,5,9,12,13]. The three goals in designing RF PCBs for electrical performance and signal integrity are:

IJIRSET

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

i) The PCB should be immune to interference from other systems.
ii) It should not produce emissions that cause problems for other systems.
iii) It should demonstrate the desired signal quality.

When electromagnetic waves get into a given PCB system, it is referred to as electromagnetic interference (EMI). On the flip side, this PCB system can also be a source of EMI and cause problems for other systems. The ability for systems to work together effectively is termed as electromagnetic compatibility (EMC). Proper layout of a PCB can greatly reduce EMI and improve EMC [6].The method by which systems and circuits interfere with each other is inductive and capacitive coupling of their related electromagnetic fields. In the 1820s Faraday and Henry showed that an electric current could be produced in a conductor by changing the current in another nearby conductor. And years later Maxwell showed that changing electric fields also produce magnetic fields. These fields are the source of many woes in PCB designs [6, 12, 13].

A.BASIC CONCEPTS OF RF PCB DESIGN

There are four areas for electrical considerations when designing and routing RF PCBs namely [2,9]: Component placement,PCB layout stack-up, Continuity of the return path that is tightly coupled to the RF traces (Ground plane) and the embedded antenna placement considerations.

B.PROPER COMPONENT PLACEMENT FOR ELECTRICAL CONSIDERATIONS

It is important for one to consider component placement with electrical performance and PCB manufacturability in mind. Usually these two goals complement each other but occasionally they conflict. When conflicts do occur an attempt should be made to resolve the conflict in a way that is mutually beneficial. If that is not possible, electrical considerations usually have priority over mechanical considerations unless doing so will result in mechanical failure of the PCB board.PCBs can be designed for analog circuits, digital circuits or mixed signals. Since analog circuits are susceptible to noise, the goal is usually to place the parts to minimize the possibility of degrading the signals. This usually means keeping the components as close as possible so that the traces can be as short as possible and keeping the signal path as straight as possible[2,9,11].

C.MULTI-LAYER PCB STACK-UP PLANNING

For EMC performance consideration, once the working frequency in mobile device product is over 5MHz, or the rise-up/fall-down time of digital signals is less than 5ns, then multi-layer PCB should be considered. The more common multi-layer PCB structure are 4-layers,6-layers and 8-layersPCB.Thus, if a product is designed using multi-layer PCB technology, then the stack-up design of these multi-layer PCBs will become very important[5,11].Planning the multi-layer PCB stack-up configuration is one of the most important aspects in achieving the best possible performance of a product. A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission increasing emissions and crosstalk and can also make the product more susceptible to external noise. These issues can cause intermittent operation due to time glitches and interference dramatically reducing the products performance and long term reliability [11,13,14].In contrast, a properly built PCB substrate can effectively reduce electromagnetic emissions, crosstalk and improve the signal integrity providing a low inductance power distribution network. And, looking from a fabrication point of view, can also improve manufacturability of the product. Suppressing the noise at the source rather than trying to elevate the problems one the product has been built makes sense.

D.GROUND PLANE REQUIREMENT FOR RF PCB DESIGN

Return currents on RF PCB designs follow the path of least impedance. If the ground plane, which is normally the return path, the return current paths may become larger leading to higher spurious emission .In addition, divided ground planes add undesirable inductance leading to poor RF performance.A continuous ground plane also provides for easy

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

connection to the ground by allowing one to drop vias from the RF module pads and antenna to be grounded and thus no additional traces are required to connect the RF circuitry to ground which eliminates unwanted inductance [2,9,11].

E.RF PCB DESIGN CONSIDERATIONS FOR EMBEDDED PCB ANTENNAS

Close proximity to components or housing affects the electrical performance of all antennas. When placed on a non-conductive area of the board, there should clearance of at least 5mm in all directions from metal components for maximum efficiency. A reduction in the efficiency of the antenna and a shift in tuned frequencies will be observed if these clearances are not followed. Proximity effects will also have an adverse effect on the radiation pattern of the antenna. Device housings should never be metal, polycarbonate and/or coated with EMI absorption material. Below 1mm clearance around the antenna, major issues do arise, such as antenna detuning and low radiation efficiency [1,2].

III. DUAL BAND GSM INVERTED-FL ANTENNA INTEGRATION

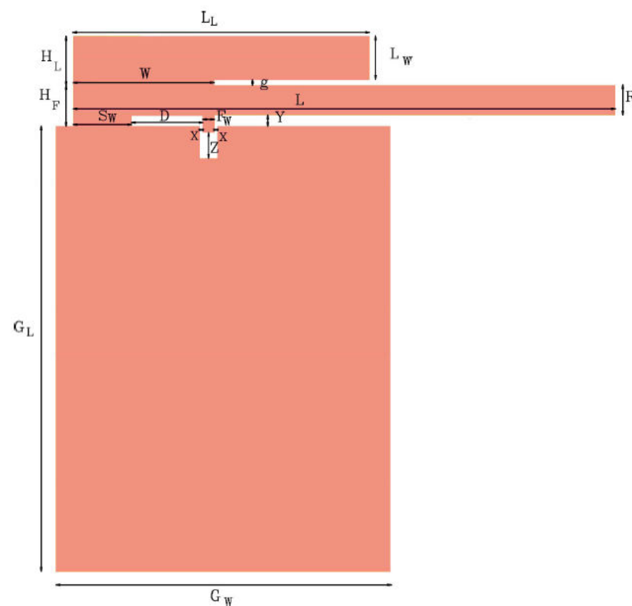


Fig 1: Printed inverted-FL antenna element

The antenna structure was designed and optimized using Agilent Advanced Design System (AADS). Its lower and upper bandwidths determined at -10dB is over 110MHz and 500MHz respectively with very low return losses of -30dB at resonant frequencies 925MHz and 1.795GHz [4].

To obtain the multitude of functions required in a smart mobile device of optimized component placement and routing is required in addition to better coupling of signal traces to return planes to minimize crosstalk and loop inductances and improved Electromagnetic Compatibility (EMC) [4]. The inverted-FL antenna design shown in Fig. 1 was integrated into an 8 layer PCB board with 4 routing layers (top, layer3, layer 6 and the bottom), two continuous ground planes (layer 2 and layer 7) and two split power planes (layer4 and layer 5).This 8 layer PCB stacking was settled upon because it achieves the objectives below:

i) Signal layers are adjacent to planes leading to small signal loop areas for reduced differential mode radiation.
ii) Signal layers are tightly coupled to their adjacent planes reducing the plane impedance (inductance) resulting in reduced common-mode radiation from cables connected to the board.
iii) Power and ground planes are closely coupled together obtaining sufficient inter-plane capacitance between the ground and power planes to provide adequate decoupling.

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

iv) High speed signals are routed on buried layers located between planes. In this way the planes act as shields and contain the radiation from the high-speed traces.
v) The PCB design utilizes multiple ground planes, which lowers the ground impedance of the board and reduces the common mode radiation.

Since the multilayer PCB is a mixed analog and digital design, there is a possibility that high-speed digital logic might interfere with the low-level analog circuits [5]. To address this legitimate concern, an understanding of the characteristics of high-frequency currents must be considered.

High frequency currents return on a plane directly underneath the signal trace, since it is the lowest impedance (lowest) inductance path. The return current, therefore, will flow on a plane adjacent to the trace regardless of the plane type. The current spreads out slightly on the plane but otherwise stays under the trace. The actual distribution is similar to a Gaussian curve in nature [10, 12]:

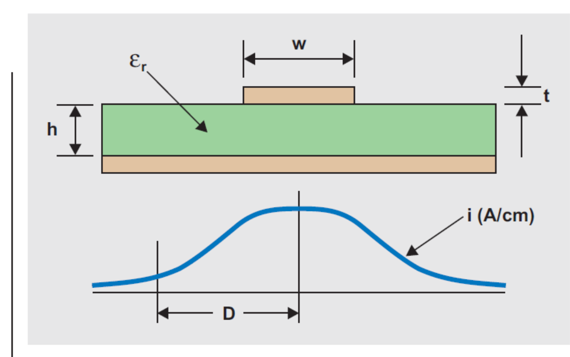


Figure 2: Distribution of high-frequency return current [10]

Figure 2 illustrates that the return current flow is directly below the signal trace. This creates the path of least impedance. The current distribution curve for the return path is defined by [10];

$$i(A/cm) = \frac{I_o}{\pi h} x \frac{1}{1+(\frac{D}{h})^2} \quad (1)$$

Whereby;
i-current distribution curve
I_o- total signal current (A)
h-height of the trace (cm)
D-distance from center of the trace (cm)

Thus it can be concluded that the digital ground currents resist flowing through the analog portion of the ground plane so will not corrupt the analog signals.

Therefore, the best approach is to use multiple ground planes and partitioning the PCB into digital and analog sections. And then analog signals must be routed only in the analog section of the board (on all layers) .Digital signals too must be routed only in the digital sections of the board (on all layers).Under this conditions, the digital return currents will not flow in the analog section of the ground plane but will remain under the digital signal traces [6].

In the design case study presented in this paper, to obtain a high routing completion rate, proper component placement and optimized routing has been done. A good component placement opens routing channels and provides space for vias. Interactive placement was done by cross-probing and dragging the components one-by-one from the schematic and placed on the PCB-taking functionality and design constraints into account. During component placement, consideration should not only be given to routing, but also to inspection and rework. An 80mil minimum clearance is required for rework tools, and an angle of 60 degrees for visual inspection. However, where possible, 45 degrees (i.e.

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

spacing between components = height of tallest component) is a good rule of thumb. Along these lines, grouping large, plated through-hole components together saves board space [14].

Similar types of components should be aligned on the board in the same orientation for ease of component identification, inspection and testing. A placement grid of 100mils is recommended for large components and 25mils for chip components. Also, similar component types should be grouped together wherever possible, with the connectivity and circuit performance requirements ultimately driving the placement [14].

A good component methodology is driven by these two objectives; minimization of track lengths and maximization of routability. Assuming d_i is the total track length estimated for each circuit and N_d the total estimated track length of the layout then;

$$\Sigma_{all\ circuits} d_i = N_d (2)$$

Thus an objective for a good PCB routing discipline should be to route tracks such that N_d is minimized.

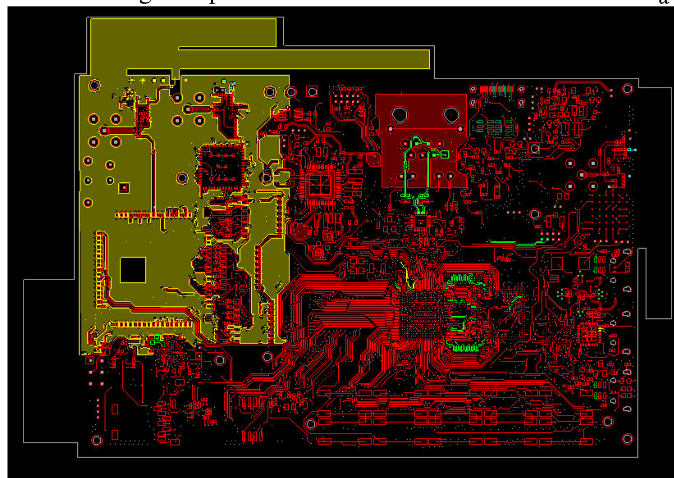


Figure 3: Top layer of the multilayer mixed analog and digital PCB design for a smart mobile device.

The RF circuitry and dual band inverted-FL PCB antenna placement and their routing was done on the top left of top layer while utilizing the continuous plane on layer two as shown in figure 2.The two layers are tightly coupled (<10mils) to reduce the crosstalk and minimize loop inductance of the RF signals being transmitted on the microstrip transmission lines done on the top layer [5].

Conductive blocking structures and other components adjoining the antenna significantly degrade radiation performance because such components serve as electromagnetic EM field scatterers and create unwanted parasitic inductance and capacitance [7]. Figure 3 above also shows the suitable location selected for the antenna on the PCB board.

The DXF import feature of Agilent Advanced Design System (AADS) momentum facilitated the designed PCB shown in Figure 1 above to be imported into the routed PCB with components., along with all nets, power and ground planes and all various components on the PCB board for electromagnetic simulation was done to determine how the embedded antenna performs in a more realistic environment [8]. Figure 4 is the top layer of the PCB imported into AADS momentum ready for electromagnetic simulation.

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

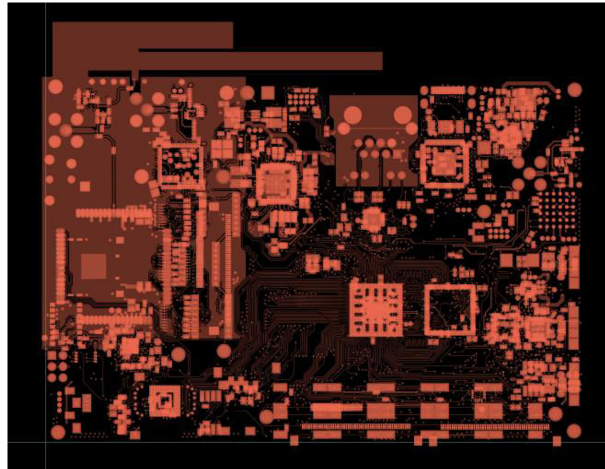
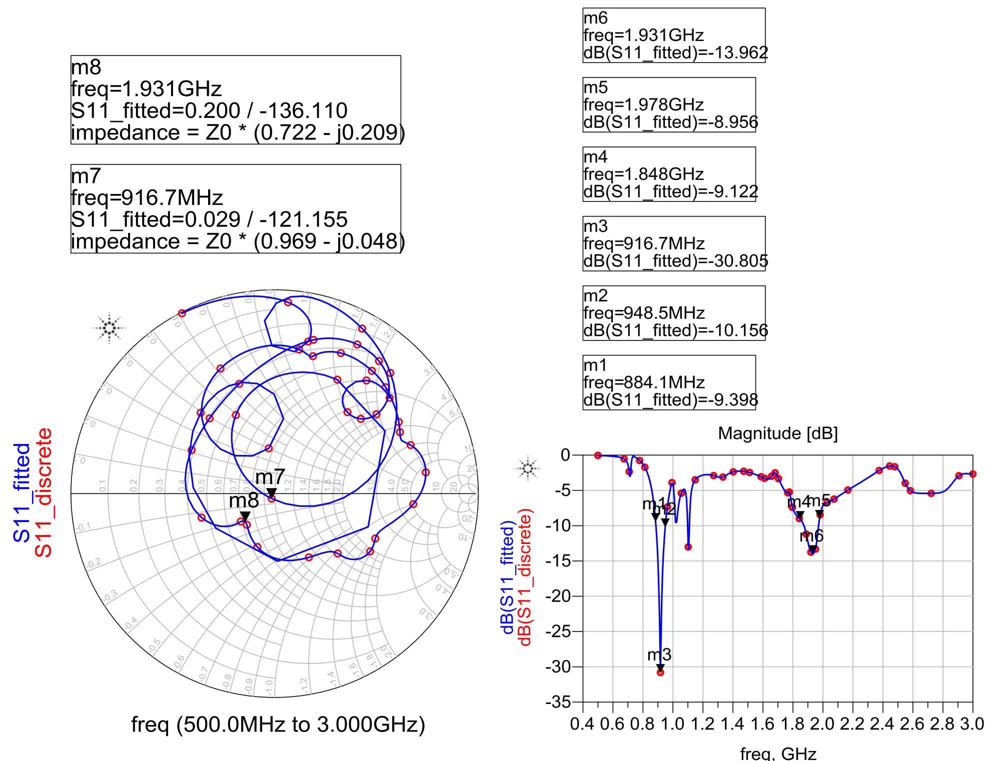


Figure 4: Top layer of the multilayer mixed analog and digital PCB design imported into Advanced Design (ADS) momentum

IV. EMBEDDED ANTENNA SIMULATION RESULTS

The simulated results for the embedded PCB-PIFL antenna are presented in figures 5 and 6 below. Using markers m7 and m8 (see figure 5), it is evident that the antenna is detuned more on the higher band compared to the lower band. From figure 6 too, it can be deduced that there is a reduction in antenna's lower bandwidth compared to the higher bandwidth. Using markers m1, m2, m3 and m4, the antenna's lower and upper bandwidths are 64MHz and 130MHz respectively.



ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

Figure 5: Simulated input impedance of the embedded antenna into a populated PCB board

Figure 6: Simulated return loss of the embedded antenna into a populated PCB board

V. DISCUSSION

An antenna is a function of its environment. Unlike most components that can be used in a design with an expected effect on the circuit, an antenna is affected by everything around. This is because the radiated electromagnetic fields from the antenna interact with nearby component which shifts its resonant frequency. This detuning is evident from figures 5 and 6 above. Integrating an antenna into a populated PCB board led to etching of its coplanar ground plane due to mounting holes, PCB tracks as its evident from figures 3 and 4. An etched ground plane ultimately changes the antenna's surface current distribution and consequently its impedance due to non-uniformity and non-continuity of the etched ground plane. Moreover, new parasitic resonant frequencies emerge as well as shown in figure 6. The number of these parasitic resonant frequencies depend on how much the ground plane is etched out and the clearance of any material and other components around the antenna area. From figure 6, a few parasitic resonant frequencies were obtained due to the optimized routing and careful selection of component selection placement around the antenna area. It is evident also from figure 6 that the change of the continuity and uniformity of the ground plane affected the bandwidth of the antenna's lower band (GSM-900) more than the higher band (GSM-1800). This is because the higher band requires a much smaller co-planar ground plane compared to the lower band, which is logical since the wavelength at GSM-1800 band is estimated to be half of the GSM-900 band.

VI. CONCLUSION

In this design case study of a smart mobile device a GSM dual band inverted-FL has been integrated into a populated multilayer mixed-signal PCB board and its performance evaluated through electromagnetic simulation. Good PCB stacking, effective PCB partitioning, proper component orientation and placement, routing discipline combined with right selection of antenna location are the keys to successful integration of PCB-PIFL into a mixed signal multilayer PCB., Improved continuity and uniformity of PCB-PIFL antenna's co-planar ground plane improves the overall performance. Good multilayer PCB stacking, is an important factor in determining the Electromagnetic Compatibility (EMC) of a product, it is effective in reducing radiation from the loops of the PCB (differential-mode emission), as well as the cables attached to the board (common-mode-emission). Proper component orientation and placement ease component identification, inspection and testing. Effective PCB partitioning and discipline in routing minimizes track lengths. Moreover, a properly done layout ensures that digital currents remain in the digital section of the board and will not interfere with analogue signals. Finally, a good antenna location selection facilitates easier antenna tuning and minimizes interference. Though a slight antenna detuning is evident, the results obtained show that the lower and upper bandwidths determined at -10dB is over 60MHz and 130MHz with return losses -30dB and -14dB at resonant frequencies 915MHz and 1.931MHz.

ACKNOWLEDGEMENT

I would like to sincerely thank Prof. Mwangi Mbuthia for his continuous guidance throughout the whole allocated period of my research. May God bless you abundantly.

REFERENCES

[1] Robert Thorpe, "The challenges of antenna integration",Antenova Limited.
[2] Freescale Semiconductor, "Compact Integrated Antennas," Application note,AN2731, December 2012.
[3] Texas Instruments, "Bluetooth Antenna Design", Application Note,AN1811,2013.
[4] Segera Davies ,Mwangi Mbuthia, "Design and Optimization of A Mobile Device PCB-PIFL Multiband Antenna for GSM Applications," IJIREST, vol. 4, no. 10, pp. 9522-9528, Oct. 2015.
[5] Barry Olney,"Multilayer PCB Stackup Planning",February 2011.
[6] Kraig Mitzner,.: Elsevier Inc., 2007, ch. 6, pp. 109-164.
[7] Richard Wallace, "Antenna Selection Guide", Application Note AN058,2012.
[8] Agilent, Advanced Design System inbuilt manual.
[9] Rick Hartley, RF/Microwave PC Board Design and Layout,L-3 Avionics Systems.

ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 11, November 2015

[10] Shridhar More Sanjay Pithadia, "Grounding in Mixed-Signal Systems Demystified,Part 1," Analog Applications Journal, pp. 1-4,2013.
[11] H. W. Ott, "Partitioning and Layout of a Mixed-Signal PCB," Printed Circuit Design, pp. 8-11, June 2001.
[12] Shridhar More ,Sanjay Pithadia, "Grounding in Mixed-Signal Systems Demystified,Part 2," Analog Applications Journal, pp. 5-8,2Q 2013.
[13] Barry Olney, "Beyond Design: Introduction to Board Level Simulation and the PCB Design Process," The PCB Design Magazine, pp.18-24, December 2012.
[14] Barry Olney, "Beyond Design: Interactive Placement and Routing Strategies," The PCB Design Magazine, pp. 12-18, December 2012.

BIOGRAPHY

Eng. Prof. Mwangi Mbuthia was born in Nyeri, Kenya in 1952. He is an Associate Professor in the School of Engineering at the University of Nairobi. He received a B.Sc.(First Class Honours) in Electrical and Electronic Engineering in 1976 from the University Nairobi, An M.Sc. and DIC in 1978 from Imperial College of Science Technology and Medicine in London, and a Ph.D in 1985 from the University of Manchester in England.In 1976 to 1977, he was a graduate engineer trainee with Kenya Power and Lighting Company. In 1978, he joined the University of Nairobi as a lecturer in the Electrical and Electronic Engineering department, rising to Senior Lecturer in 1988. In 1994 he left the University and founded Elcom Systems Ltd. a company providing specialized hardware and software solutions for the telecommunication sector. As the CEO of Elcom Systems Ltd. he has developed and deployed several specialized telecommunication hardware and software solutions for many private and public sector companies and institutions.In 2000, he rejoined the University of Nairobi and he is currently the Dean, School of Engineering. He is a Professional Engineer, a chartered Engineer in United Kingdom and a Member of IEEE.He is the author of more than 30 articles and has created over 15 inventions under Elcom Systems Ltd. His research interests include broadband last mile connectivity devices, special materials and devices for solar power applications, internet of things devices, energy delivery automation and smart grids.

Davies Rene Segera was born in Nyamira,Kenya in October 30, 1988.He received his BSc. Degree in electrical and Information Engineering from the University of Nairobi,Kenya in 2013, where he is currently working towards the MSc. degree in Electrical and Information Engineering. His research interests include embedded systems design, Embedded antenna design, Robotics and compiling Linux images for embedded devices.